SIMULATION OF EXASCALE NODES THROUGH RUNTIME HARDWARE MONITORING

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9/18/2013

CHALLENGES OF EXASCALE NODE RESEARCH

MANY DESIGN DECISIONS

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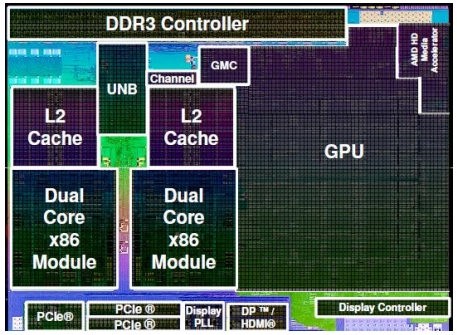
Heterogeneous Cores



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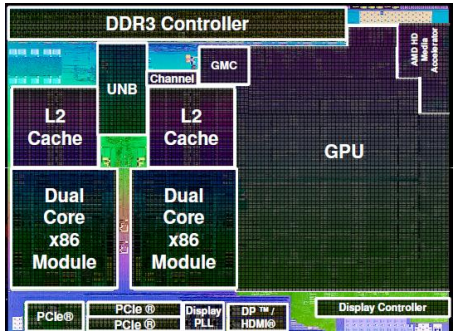

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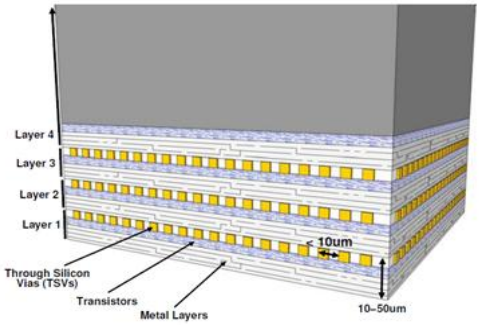

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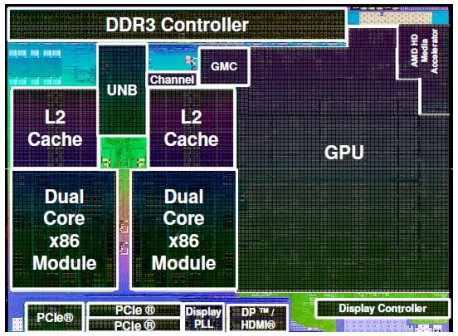

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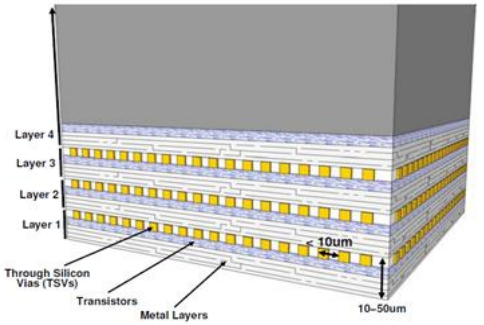

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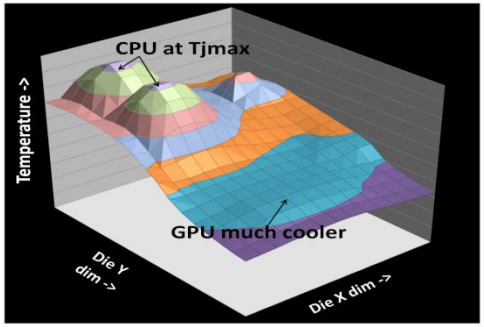

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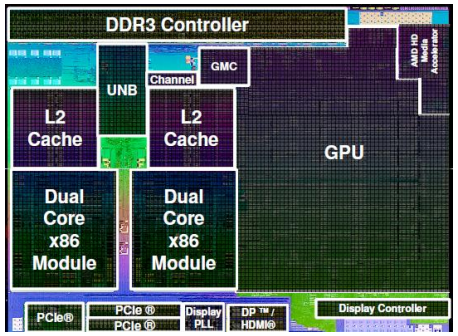

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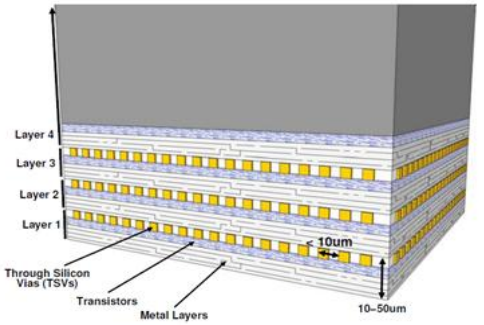

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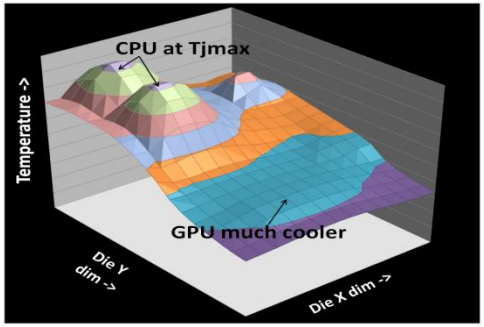

Power Sharing? Heat dissipation? Sprinting?

Software Co-Design

```
Real_t vol = volo[i]*vnew[i] ;
Real_t norm = (Real_t)(1.0) / ( vol + ptiny ) ;

Real_t dxj = (Real_t)(-0.25)*(SUM4(x0,x1,x5,x4) - SUM4(x3,x2,x6,x7)) ;
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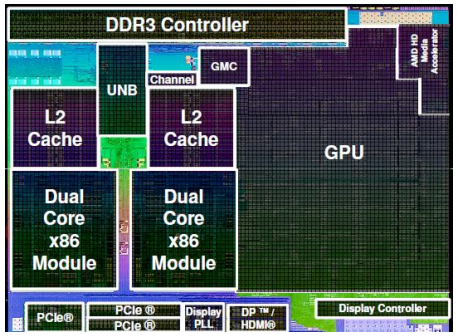

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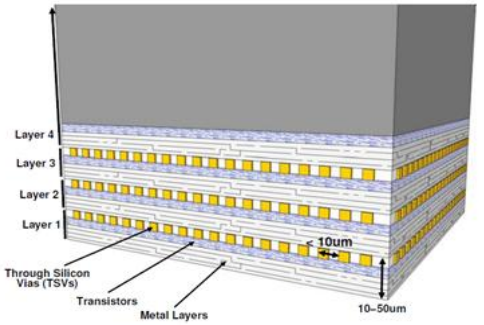

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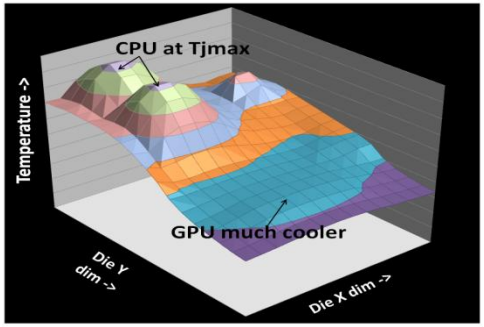
Exascale: Huge Design Space to Explore



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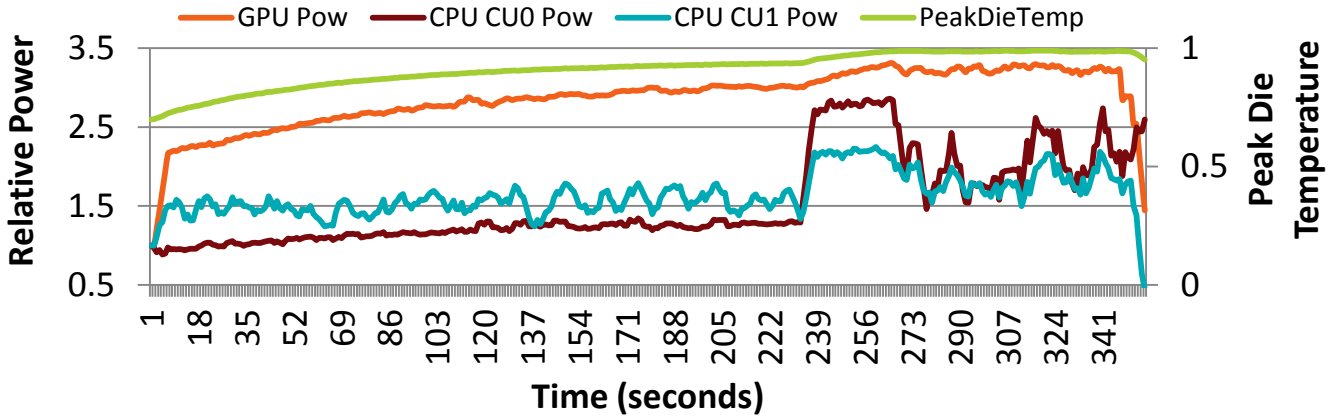
INTERESTING QUESTION REQUIRE LONG RUNTIMES

- Power and Thermals on a real heterogeneous processor:



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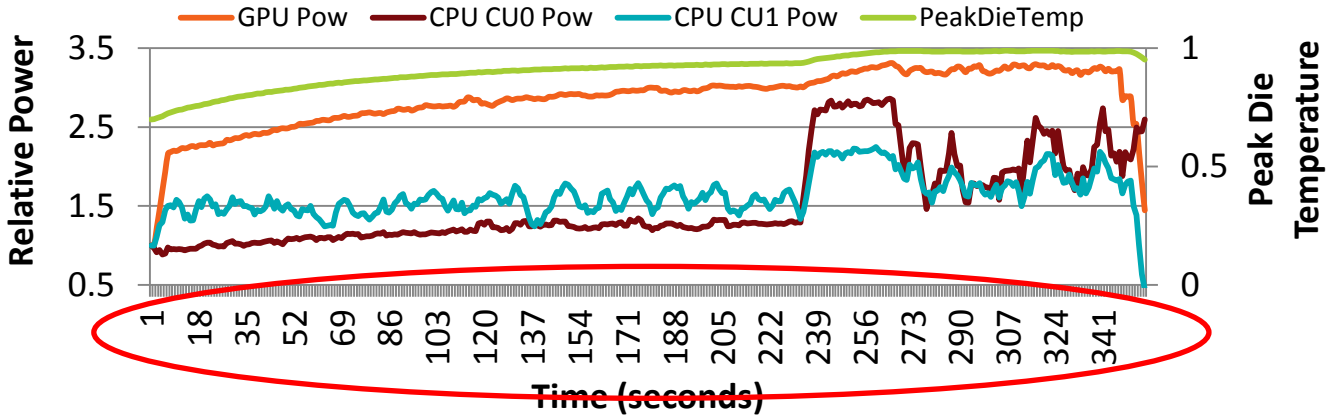

– ~2.5 trillion CPU instructions, ~60 trillion GPU operations

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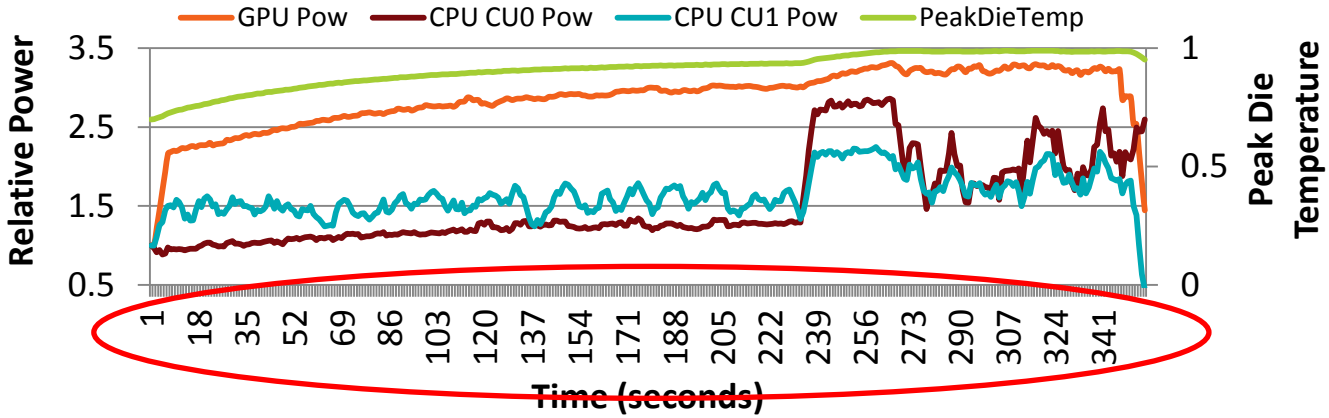

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  - Large initialization phases, many long iterations
  - Not microbenchmarks
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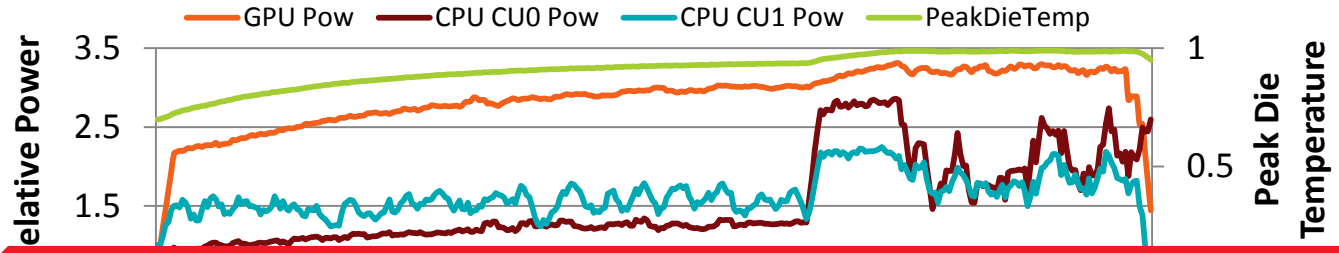

Exascale: Huge Execution Times

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EXISTING SIMULATORS

AMD

- Microarchitecture Sims: e.g. gem5, Multi2Sim, MARSSx86, SESC, GPGPU-Sim
  - Excellent for low-level details. We need these!
  - Too slow for design space explorations: **~60 trillion operations = 1 year of sim time**
- Functional Simulators: e.g. SimNow, Simics, QEMU, etc.
  - Faster than microarchitectural simulators, good for things like access patterns
  - No relation to hardware performance
- High-Level Simulators: e.g. Sniper, Graphite, CPR
  - Break operations down into timing models, e.g. core interactions, pipeline stalls, etc.
  - Faster, easier to parallelize.
  - Runtimes and complexity still constrained by desire to achieve accuracy.

TRADE OFF INDIVIDUAL TEST ACCURACY

AMD

- Doctors do not start with:

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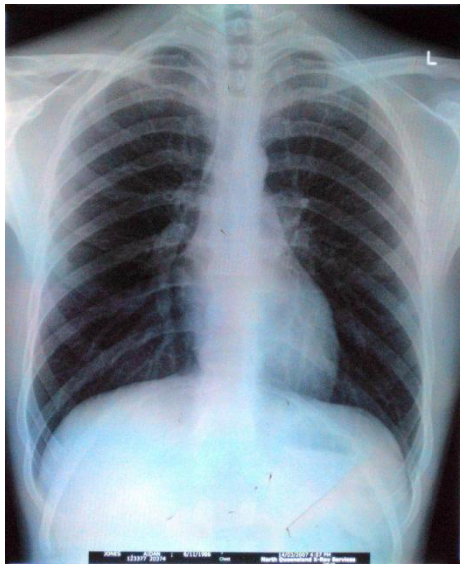

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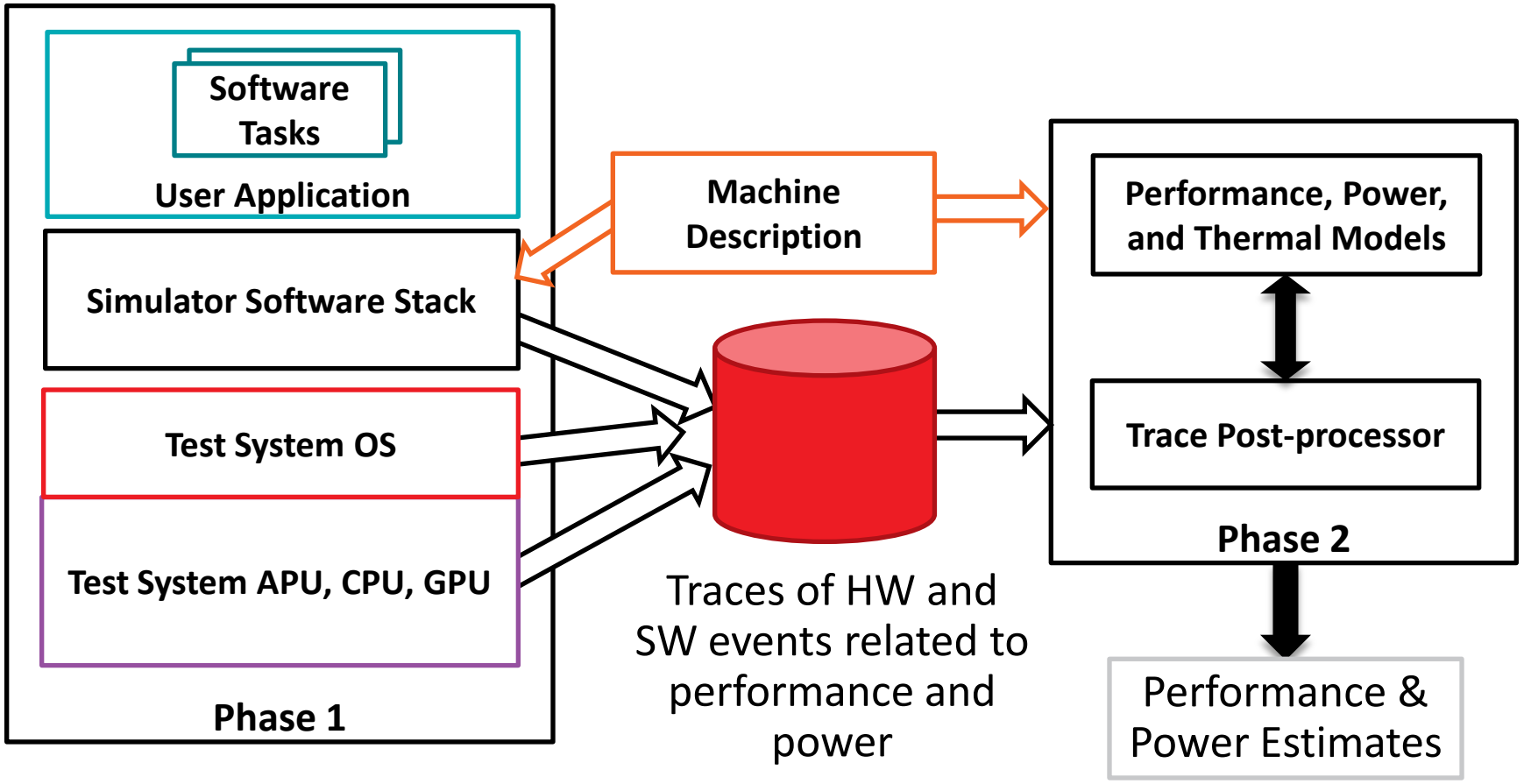
Fast Simulation Using Hardware Monitoring

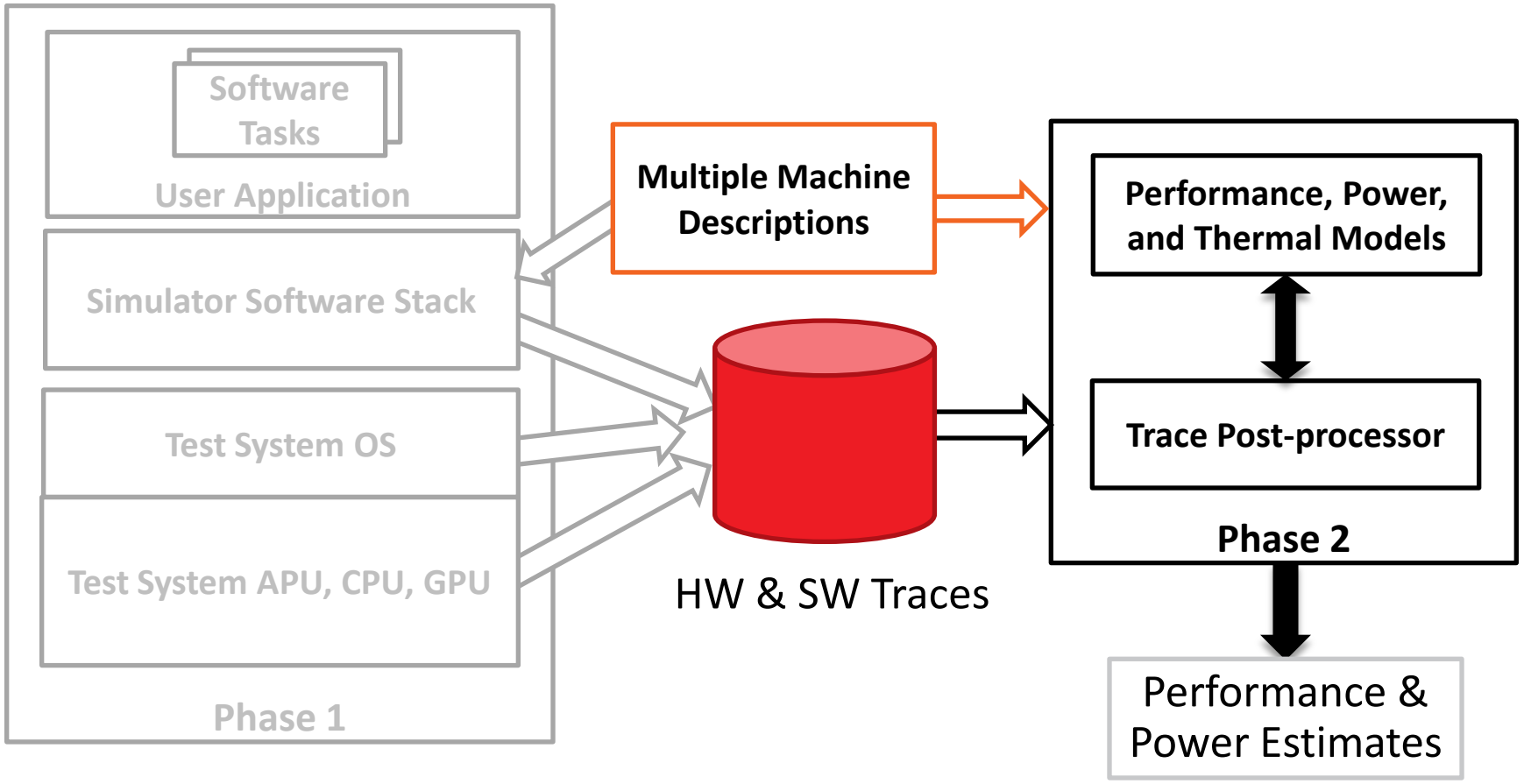
HIGH-LEVEL SIMULATION METHODOLOGY

MULTI-STAGE PERFORMANCE ESTIMATION PROCESS



BENEFITS OF MULTI-STEP PROCESS

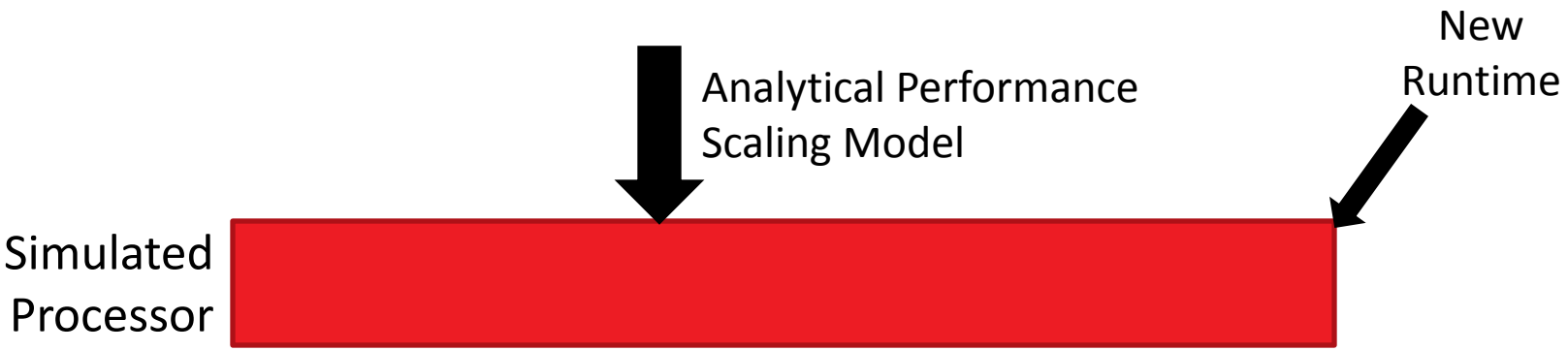
MANY DESIGN SPACE CHANGES ONLY NEED SECOND STEP



PERFORMANCE SCALING A SINGLE-THREADED APP

Gather statistics and performance counters about:

- Instructions Committed, stall cycles
- Memory operations, cache misses, etc.
- Power usage



ANALYTIC PERFORMANCE SCALING

AMD

- CPU Performance Scaling:
  - Find stall events using HW perf. counters. Scale based on new machine parameters.
  - Large amount of work in the literature on DVFS performance scaling, interval models..
  - Some events can be scaled by fiat:
    "If IPC when not stalled on memory doubled, what would happen to performance?"

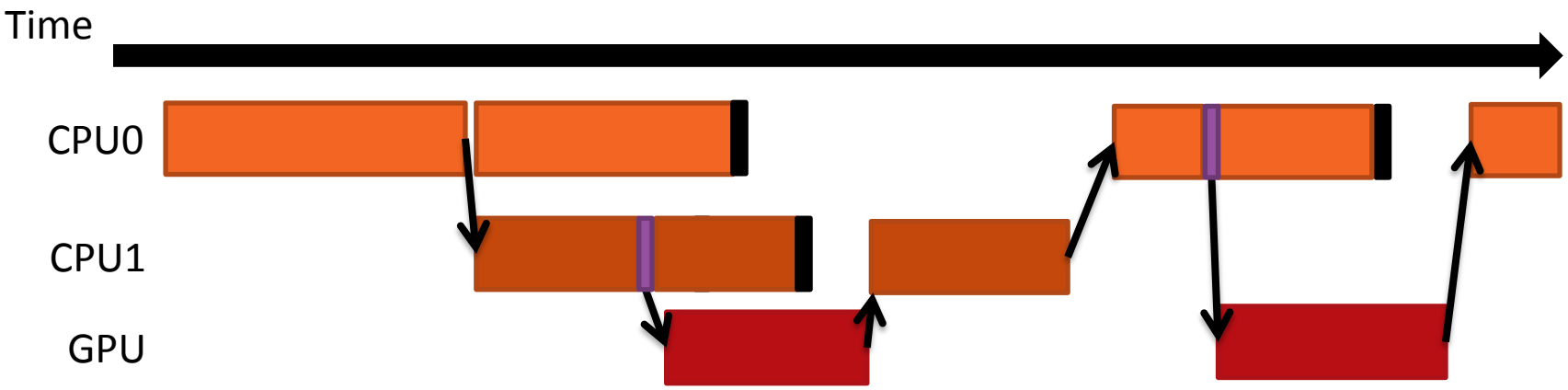
- GPU Performance Scaling:
  - Watch HW perf. counters that indicate work to do, memory usage, and GPU efficiency
  - Scale values based on estimations of parameters to test

OTHER ANALYTIC MODELS

AMD

- Cache/Memory Access Model
  - Observe memory access traces using binary instrumentation or hardware
  - Send traces through high-level cache simulation system
  - Find knees in the curve, feed this back to CPU/GPU performance scaling model
- Power and thermal models
  - Power can be correlated to hardware events or directly measured
  - Scaled to future technology points
  - Any number of thermal models will work at this point
- Thermal and power models can feed into control algorithms that change system performance
  - This is **another** HW/SW co-design point. Fast operation is essential.

SCALING PARALLEL SEGMENTS REQUIRES MORE INFO



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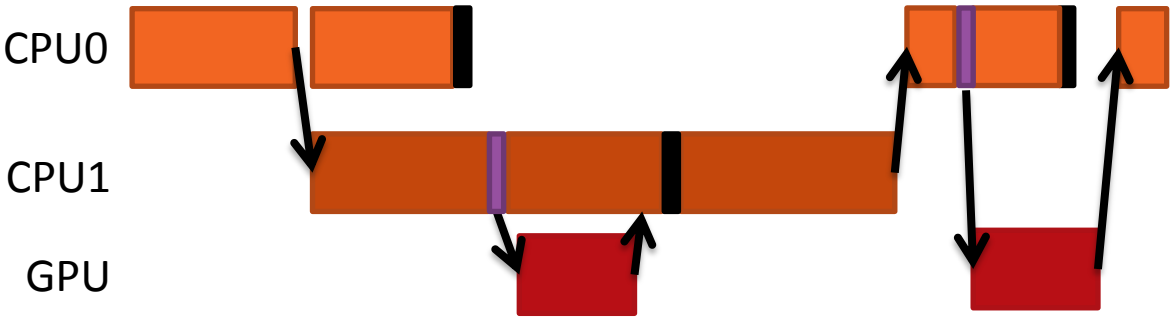

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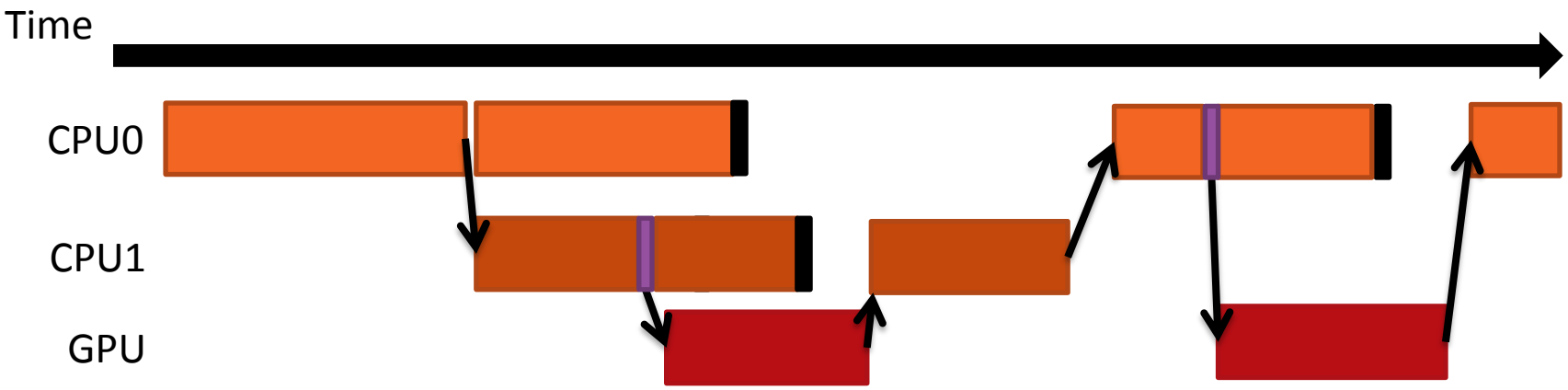

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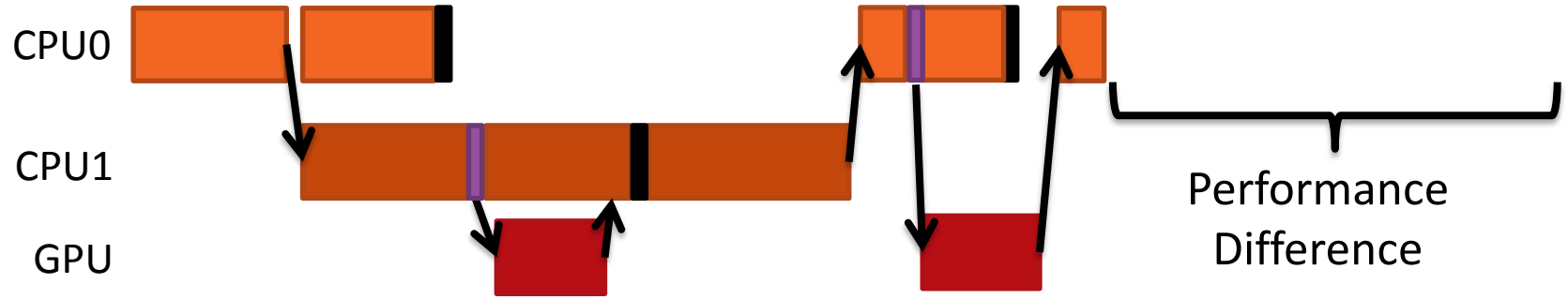

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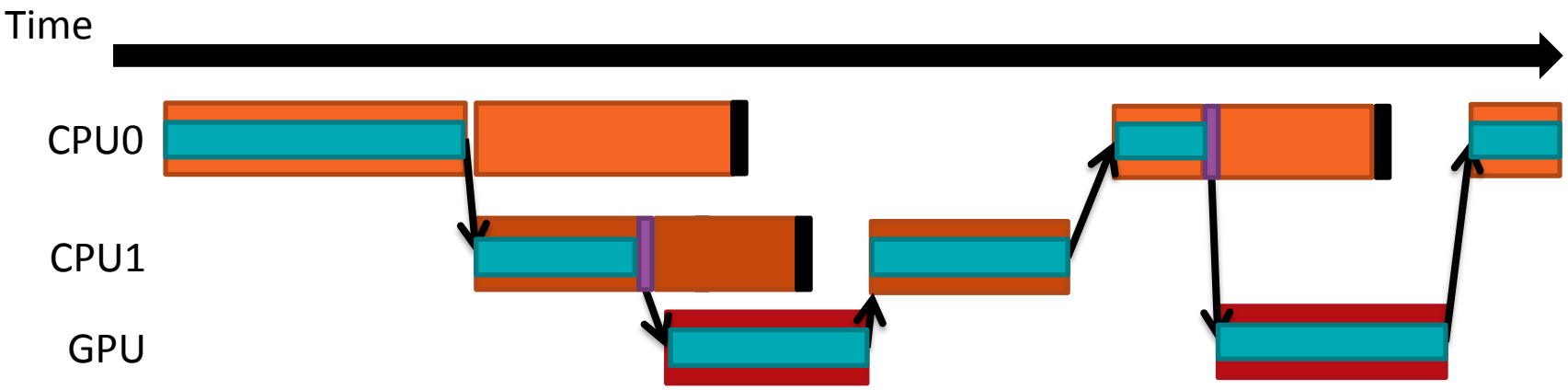

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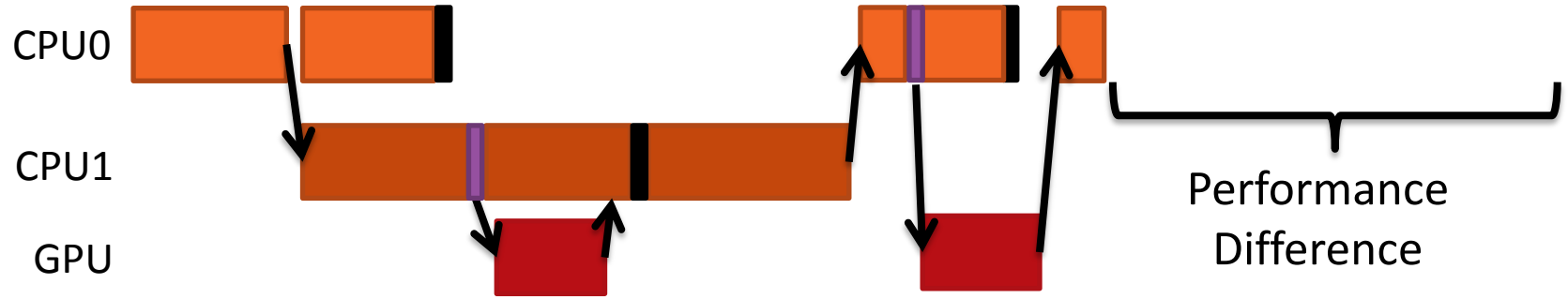

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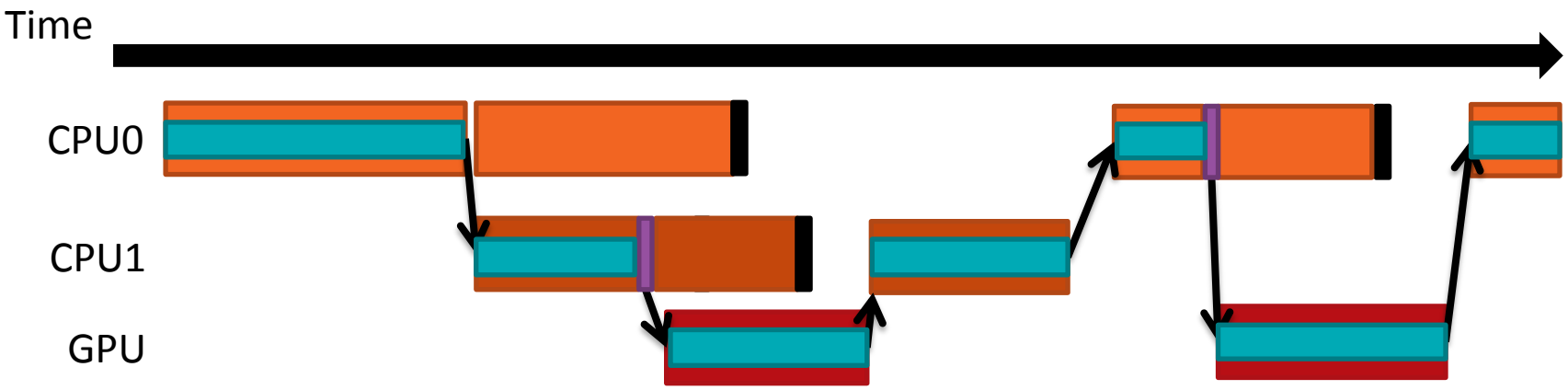

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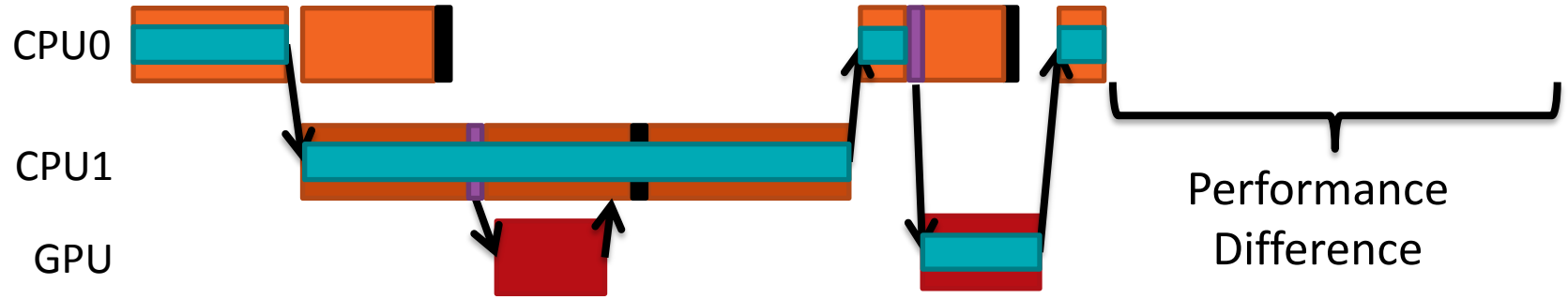
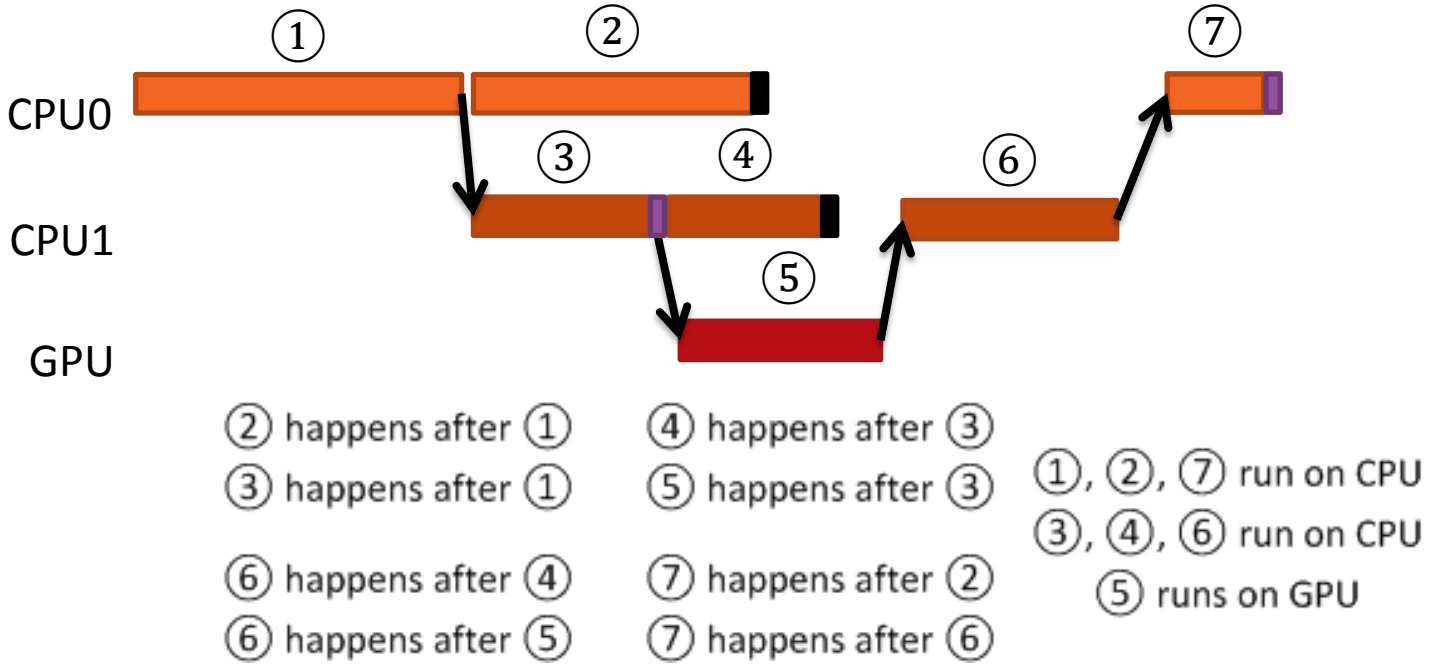


MUST RECONSTRUCT CRITICAL PATHS

- Gather program-level relationship between individually scaled **segments**
- Use these happens-before relationships to build a legal execution order



- Gather ordering from library calls like pthread_create() and clWaitForEvents()
- Can also split segments based on program phases

CONCLUSION

AMD

Exascale node design space is huge

Trade off some accuracy for faster simulation

Use analytic models based on information from existing hardware

Research Related Questions

MODSIM RELATED QUESTIONS

AMD

- Major Contributions:
  - A fast, high-level performance, power, and thermal analysis infrastructure
  - Enables large design space exploration and HW/SW co-design with good feedback

- Limitations:
  - Trace-based simulation has known limitations w/r/t multiple paths of execution, wrong-path operations, etc.
  - It can be difficult and slow to model something if your hardware can't measure values that are correlated to it.

- Bigger Picture:
  - Node-level performance model for datacenter/cluster performance modeling
  - First pass model for APU power sharing algorithms.
  - Exascale application co-design
  - Complementary work to broad projects like SST

MODSIM RELATED QUESTIONS

AMD

- What is the one thing that would make it easier to leverage the results of other projects to further your own research
  - Theoretical bounds and analytic reasoning behind performance numbers. Even “good enough” guesses may help, vs. only giving the output of a simulator

- What are important thing to address in future work?
  - Better analytic scaling models. There are a lot in the literature, but many rely on simulation to propose new hardware that would gather correct statistics.
  - It would be great if open source performance monitoring software were better funded, had more people, etc.

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Backup

AN EXASCALE NODE EXAMPLE QUESTION

AMD

- Is 3D-Stacked Memory Beneficial for Application X?

Baseline Performance
Bandwidth Difference
Latency Difference
Thermal Model
Core Changes due to Heat

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Performance results based on design point(s)

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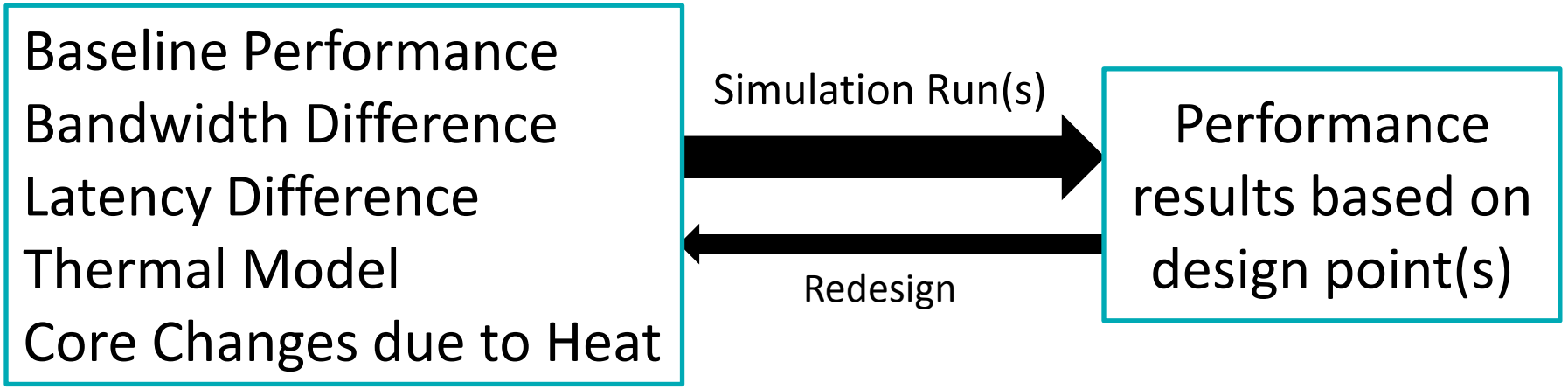

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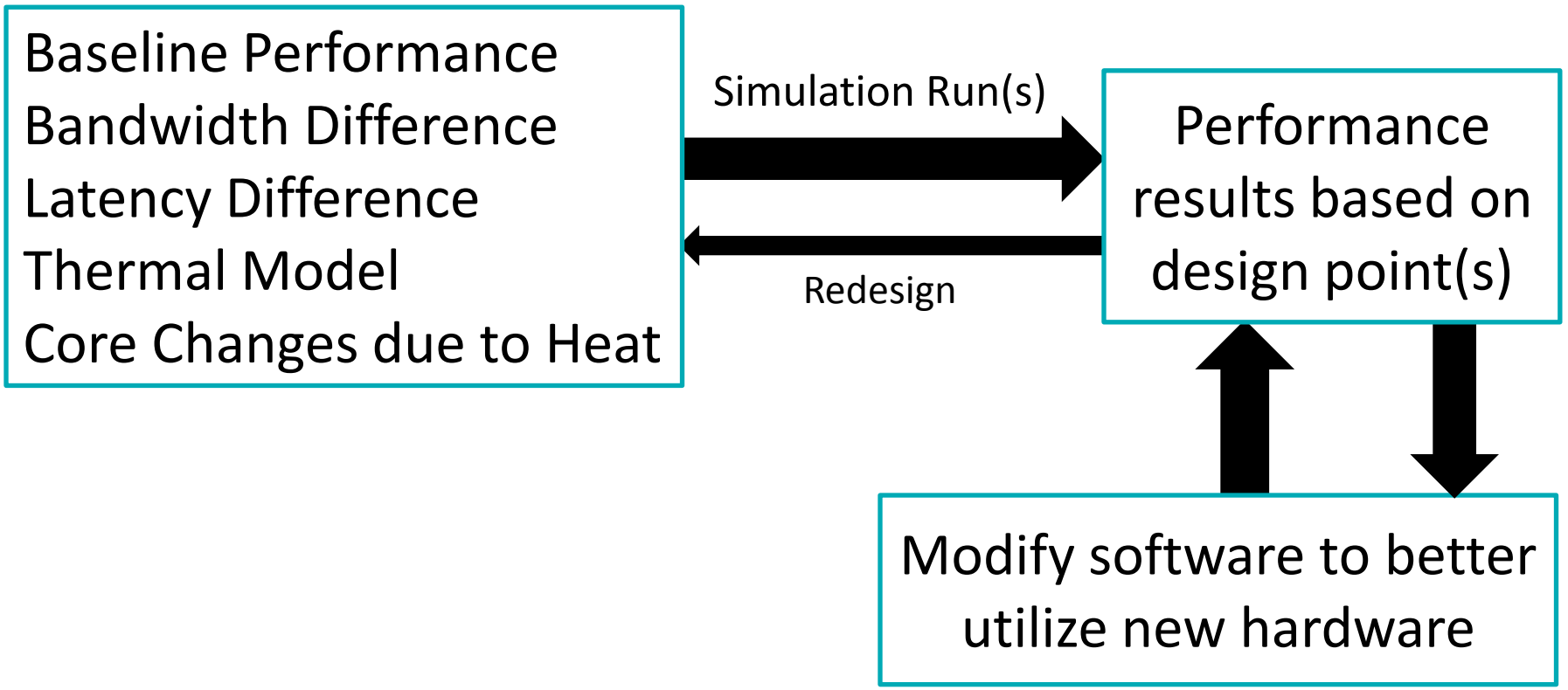

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