JOSEPH LEE GREATHOUSE

Austin, TX • joseph.l.greathouse@gmail.com

Experience

Advanced Micro Devices, Inc. **Fellow** **Aug. 2012 – Present**

- Software architect for AMD's Instinct GPUs, handling the design of HW, FW, and SW interactions
  - Co-designed multiple HW features, including coherence, performance monitors, TLBs, and RAS
  - Led debug, workaround development, and customer communication for multiple hardware issues
  - Created training materials on AMD HW & SW; delivered training to internal and external customers
- Performance engineer responsible for optimizing SW, HW, and FW for GPU compute solutions
  - Designed, implemented, and published new GPGPU algorithms, including for sparse linear algebra
- Previously researched topics in performance and power monitoring and management in AMD Research
  - Technical lead for a team of 10 engineers and multiple interns, focusing on HW/SW interaction topics
  - Created a new simulator for AMD's exascale program based on hardware performance monitoring
- Awarded 24 US patents; 11 patent submissions pending; 25 conference and 7 workshop publications

University of Michigan **Research Assistant** **May 2007 – Aug. 2012**

- Identified methods of distributing security and correctness analyses to many users to reduce slowdown
- Managed graduate and undergraduate students through the development of prototype systems

University of Michigan **Teaching Assistant** **Jan. 2012 – Apr. 2012**

- Led discussions and evaluated projects for graduate level parallel computer architecture course

Kelly Services / Intel Corp. **Research Contractor** **May 2010 – Oct. 2010**

- Researched HW & SW approaches for improving the speed of the Intel Inspector XE data race detector

International Business Machines Corp. **Speed Team Intern** **May 2008 – Aug. 2008**

- Designed and built an InfiniBand verification suite that caught multiple bugs in IBM PowerVM firmware

University of Illinois **Teaching Assistant** **Jan. 2005 – Aug. 2006**

- Taught discussion sections and graded for undergraduate computer architecture and digital logic courses

Education

University of Michigan, Ann Arbor
Ph.D. Computer Science and Engineering — May 2012
Advisor: Prof. Todd Austin
Dissertation topic: Hardware Mechanisms for Distributed Dynamic Software Analysis

University of Michigan, Ann Arbor
M.S.E. Computer Science and Engineering — May 2008

University of Illinois at Urbana-Champaign
B.S. Computer Engineering with Honors — May 2006

Computer Languages and Software Experience

Languages: C, C++, HIP, CUDA, OpenCL, x86 assembly, AMD GCN, CDNA, and RDNA assembly, Python
Software Systems: Linux kernel, multiple AMD-internal simulation, firmware, and hardware analysis tools

Honors and Associations

Association for Computing Machinery, Sr. Member
Institute of Electrical and Electronics Engineers, Sr. Member
Eta Kappa Nu Electrical & Computer Eng. Honor Society
2016 IISWC Best Paper Award
2011 CGO Best Student Presentation Award
Tau Beta Pi Engineering Honor Society