

3D Numerical Analysis of Two-Phase Immersion Cooling for Electronic Components

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MOTIVATION

Cooling solutions for supercomputers

- Air cooling
- Water cooling
- One-phase immersion cooling
- Two-phase immersion cooling

Cooling solutions applied in Top50 Supercomputing systems [1]



[1] "Top 500 supercomputers," Top 500 list for November 2017. www.top500.org

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INTRODUCTION

Heat release

Two phase immersion cooling

Power source (CPU, GPU)

Liquid vaporization

Chilling facility

Condensing pipe

Main advantages

- High latent heat in liquid vaporization
- Less space for heat sink / cold plate
- Less cooling energy





INTRODUCTION

Research goals

- Understand impact of two-phase immersion cooling on CPU/GPU processors
- Investigate thermal coupling between nearby processors
- Obtain capable processor power
- Analyze trade-offs in supercomputing system design

Research approaches

- Numerical study in ANSYS FLUENT (current work)
- Experiment testbed

MODEL CONFIGURATION

Modeling approach



Simulation geometries in ANSYS FLUENT

Main features:

- Mimic structure in computing rack
- 4 boards, 4 or 8 processors
- Consider boiling, ignore condensing

MODEL CONFIGURATION

Dimensions and boundary conditions

Model configuration

Dimensions

Simulation zone:	15cm × 25cm × 15cm
Compute board:	7cm × 20cm
Board gap:	3.8cm
CPU package:	5cm × 5cm

Conditions

Cooling liquid:	Novec7000 & FC72
Boiling point:	34°C & 56°C
Subcooling:	No
Package power:	50W – 300W
Top of domain:	Flow outlet

MODEL CONFIGURATION

Governing equations

Mass conservation:

Momentum equation:

Energy conservation:

$$\begin{aligned} \frac{\partial \rho}{\partial t} + \nabla \cdot (\rho \vec{v}) &= 0 \\ \frac{\partial}{\partial t} (\rho \vec{v}) + \nabla \cdot (\rho \vec{v} \vec{v}) &= -\nabla p + \nabla \cdot (\bar{\tau}) + \rho \vec{g} + \vec{F} \\ \frac{\partial}{\partial t} (\rho h) + \nabla \cdot (\rho h \vec{v}) &= \nabla \cdot [(k + k_t) \nabla T] + S_h \end{aligned}$$

Turbulence model:

Standard k - ε model

Boiling model:

RPI model



MODEL VALIDATION



Conditions

Cooling liquid:	FC72
Boiling point:	56°C
Power source:	1cm × 1cm

Comparison data points near CHF

	q" (W/cm²)	ΔT _{sat} (K)
Experiment	15.7	25.2
FLUENT	14	25.9
error	10%	3%

[1] Jack L. Parker, and Mohamed S. El-Genk. "Effect of surface orientation on nucleate boiling of FC-72 on porous graphite." Journal of heat transfer 128.11: 1159-1175, 2006.

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One package on board vs. two packages on board



Time = 0.05s

Phenomenon of liquid vaporization in first 5 seconds when package power is 125W (Blue is liquid phase, red is vapor phase)

One package on board vs. two packages on board



Time = 4.90s

Phenomenon of liquid vaporization in first 5 seconds when package power is 125W (Blue is liquid phase, red is vapor phase)

One package on board vs. two packages on board



Volume fraction contour when package power is 125W (Blue is liquid phase, red is vapor phase)

- Upper packages are covered by thicker vapor
- Lower packages in "two packages" test and all packages in "one package" test are covered by thinner vapor and those thicknesses are similar

One package on board vs. two packages on board

One package Two packages 47.12 46.30 45.48 44.66 43.84 43.02 42.20 41.38 40.56 39.74 38.92 38.10 37.28 36.46 35.64 34.82 34.00 [C]

Lid temperature contour

- Hot zones appear on top central area due to insufficient liquid contact
- Temperature maps on "related" packages are similar

One package on board vs. two packages on board



Summary

 Temperature situations on different boards are almost the same

- Lower packages in "two packages" test and all packages in "one package": same temperature
- Upper packages are much hotter than lower packages

Two packages on board







Phenomenon of liquid vaporization in first 5 seconds, different power values (Blue is liquid phase, red is vapor phase)

Two packages on board





Phenomenon of liquid vaporization in first 5 seconds, different power values (Blue is liquid phase, red is vapor phase)

Two packages on board



Lid temperature contour on 2nd board from left

- When power is higher, temperature gradient on lid is bigger
- Temperature gradient on lower package is smaller

Two packages on board

Soc 2 max Soc 2 Soc 2A max Soc 2A Soc 2B max Soc 2B Temperature (°C) Temperature (°C) Socket power (W) Package power (W)

Package power and lid temperature

Package power and temperature on silicon (estimation)

- When power rises, temperature increases faster
- Assume package thermal resistance is 0.2°C/W (lid to silicon)
 - In "one package" test, highest capable package power is about 230W
 - In "two packages" test, highest capable package power is about 180W







Macro scale: Micro scale:

provide cooling solutions for computing center provide thermal info for processor design

Thank You – Questions?

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