IMPLEMENTING A LEADING LOADS PERFORMANCE PREDICTOR ON COMMODITY PROCESSORS

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How fast is your application at different CPU frequencies?

AMD
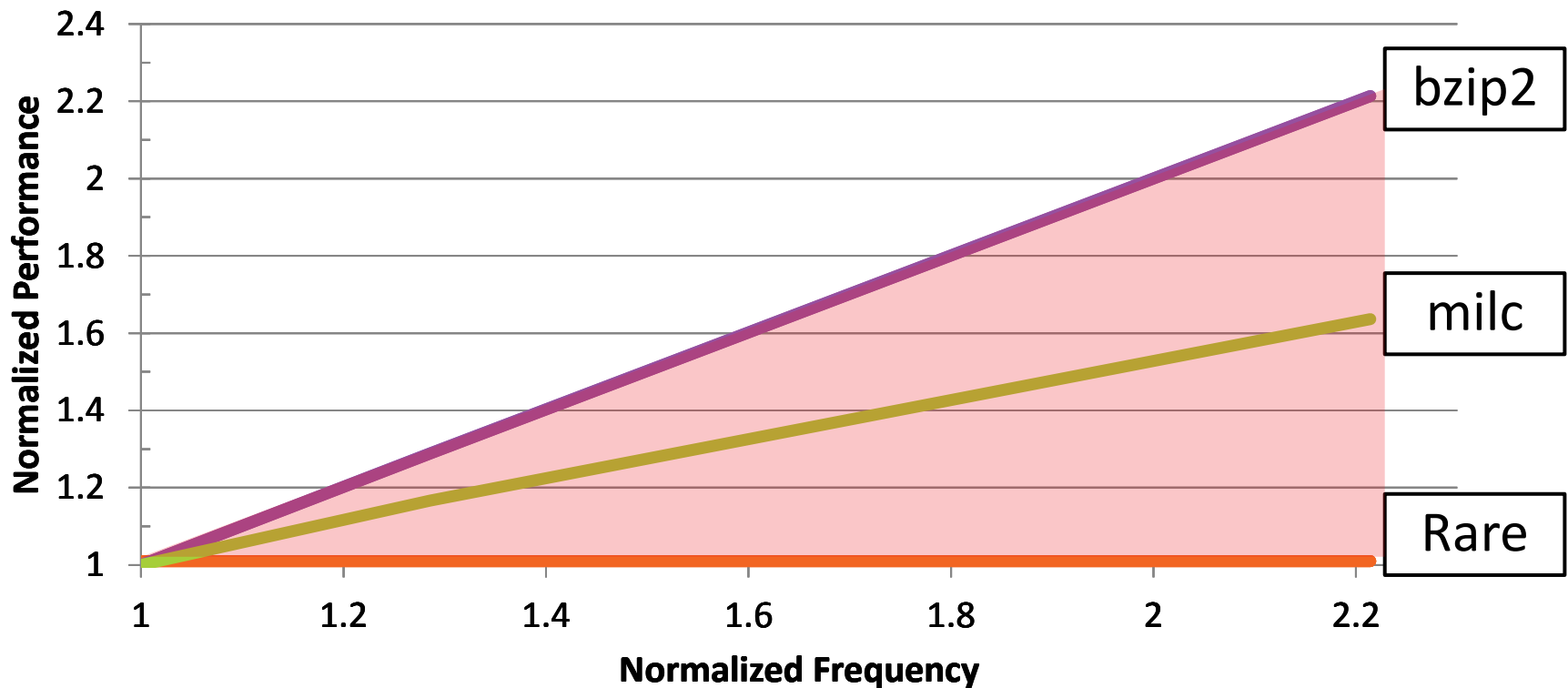
WHAT HAPPENS WHEN YOU CHANGE FREQUENCY?

AMD

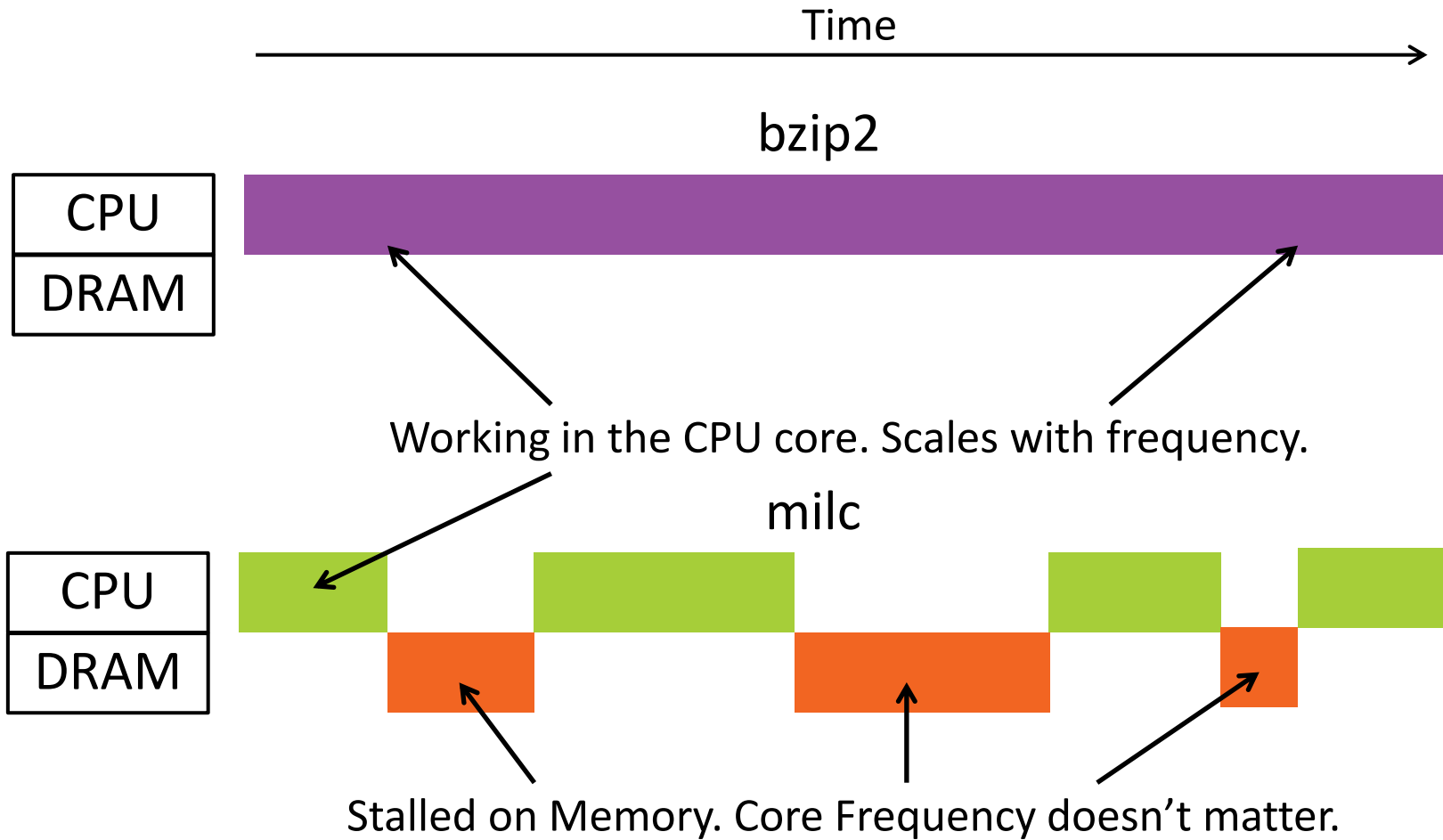| Estimate #1 | Nothing. Who cares about frequency? |
| Estimate #2 | Performance difference is equal to frequency change. |
| Estimate #3 | Something in between. |

WHY DON'T NAÏVE ESTIMATES ALWAYS WORK?

Time →

bzip2

Working in the CPU core. Scales with frequency.

milc

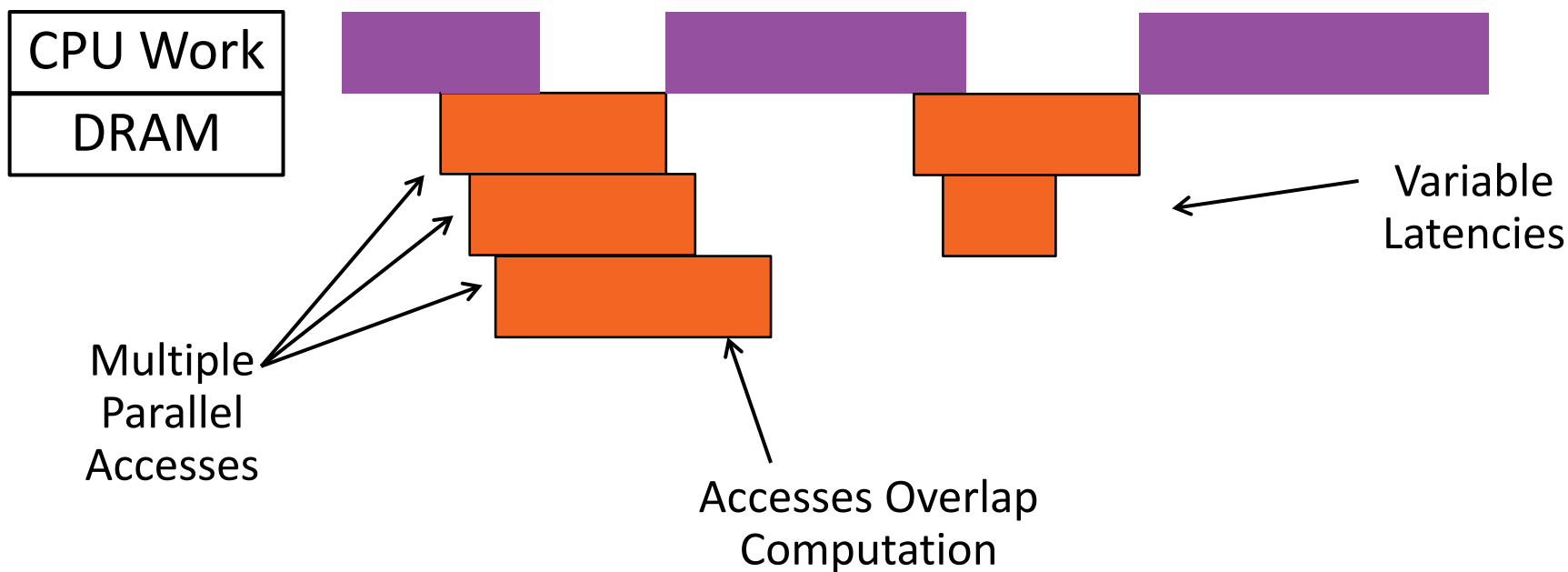Stalled on Memory. Core Frequency doesn't matter.

Core _and memory_ time both matter

HOW DO YOU ESTIMATE "MEMORY TIME"?
MODERN CORES MAKE THIS DIFFICULT

◢ Count the amount of time with an outstanding load?

◢ Count last-level cache misses?

CPU Work

DRAM

Variable Latencies

Multiple Parallel Accesses

Accesses Overlap Computation

"LEADING LOADS" MEMORY TIME ESTIMATION

Described by 3 separate groups in CF 2010, IEEE TOC, and IGCC 2011
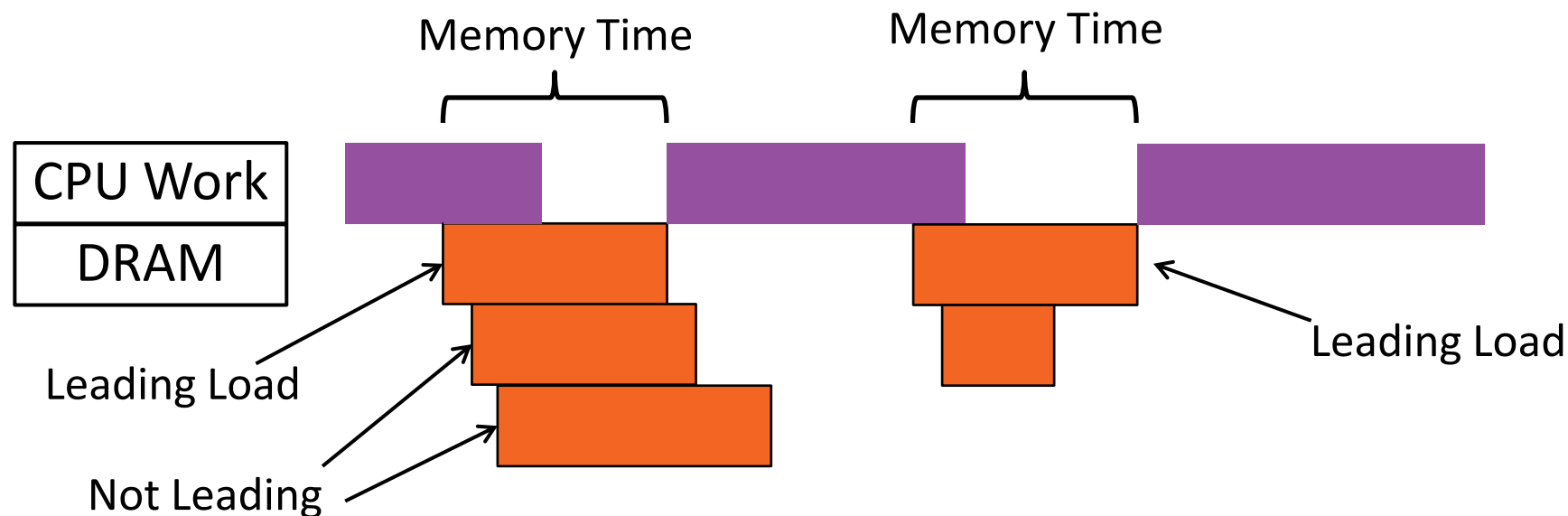
Memory time approximately time that a leading loads is active

Simulation: ~0.2% estimation error across 2x change in frequency

AMD ↗

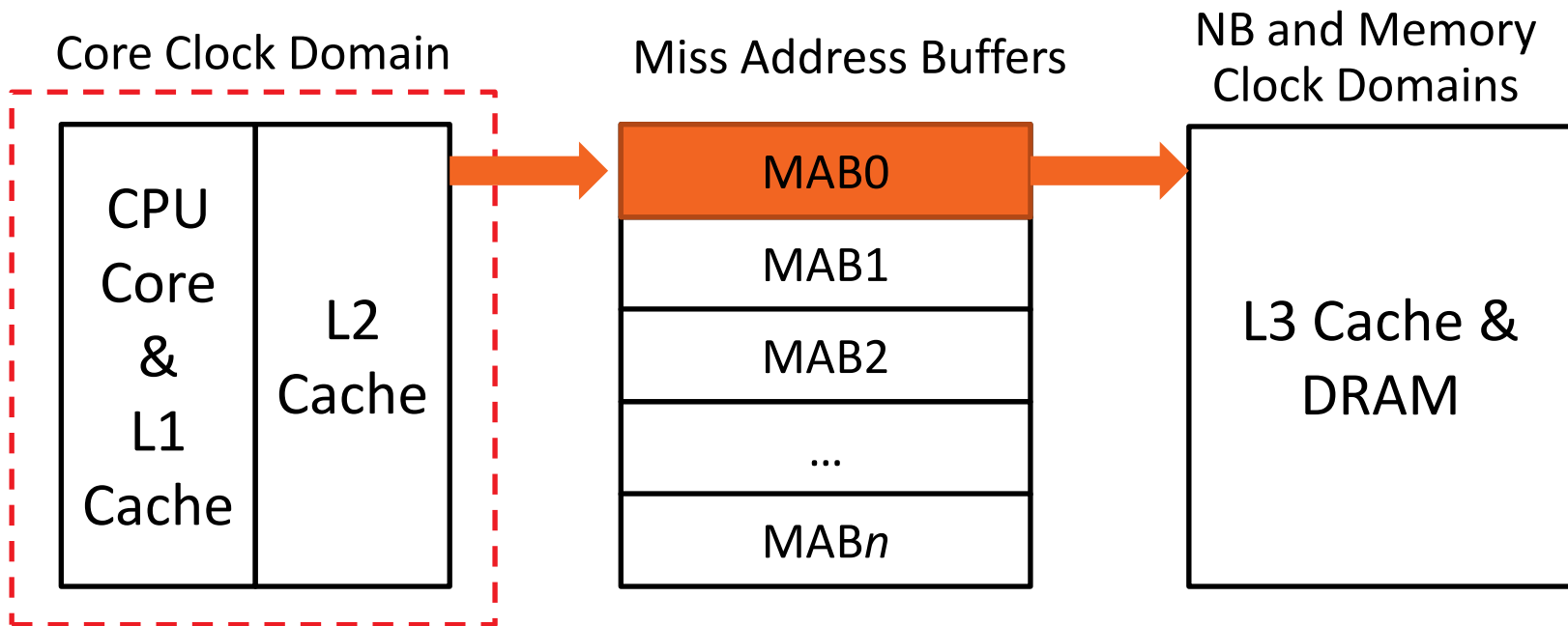## L2 cache misses held in Miss Address Buffer (MAB)

– MAB entries have a static priority (e.g. MAB0 is highest priority)

– Highest priority empty MAB holds the miss until it returns from memory

Core Clock Domain | Miss Address Buffers | NB and Memory Clock Domains

CPU Core & L1 Cache | L2 Cache → MAB0 / MAB1 / MAB2 / … / MABn → L3 Cache & DRAM

Performance event 0x69 allows SW to count # of cycles with filled MABs

LEADING LOADS ON AMD PROCESSORS

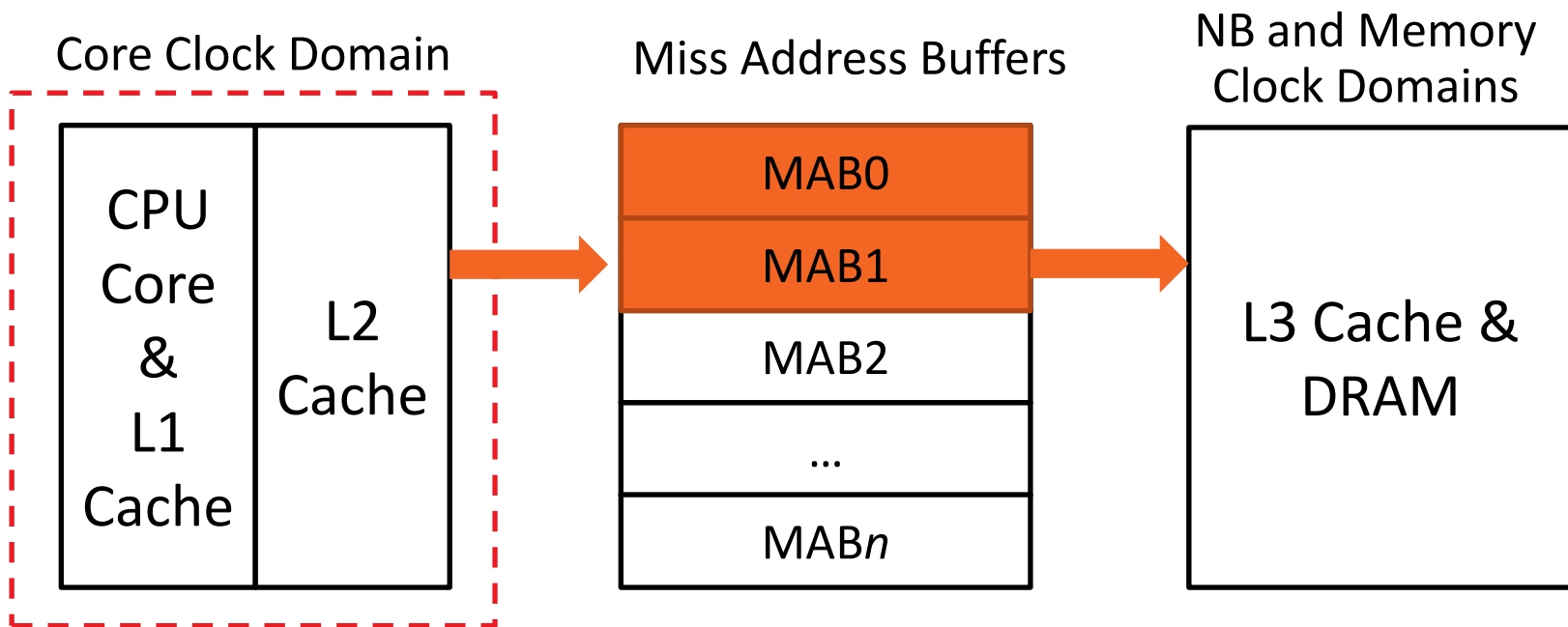**AMD**

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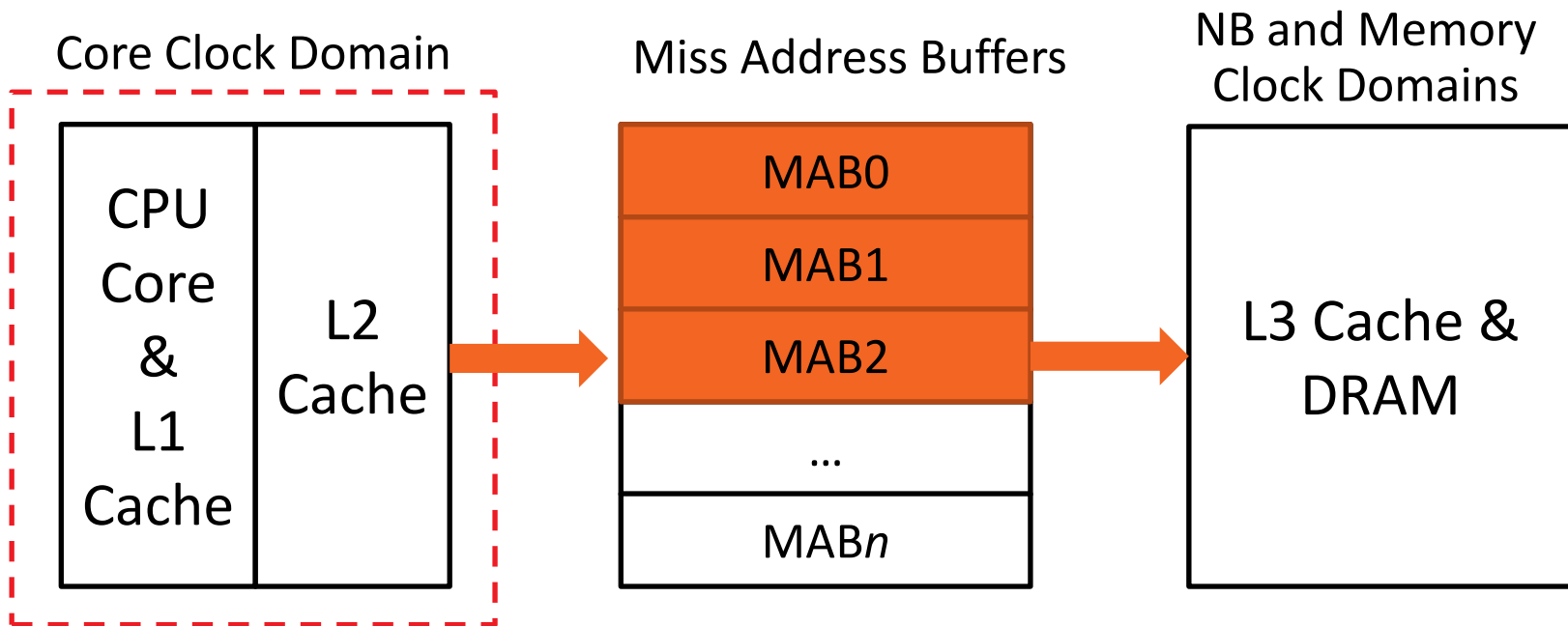**AMD**

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MAB2

...

MABn

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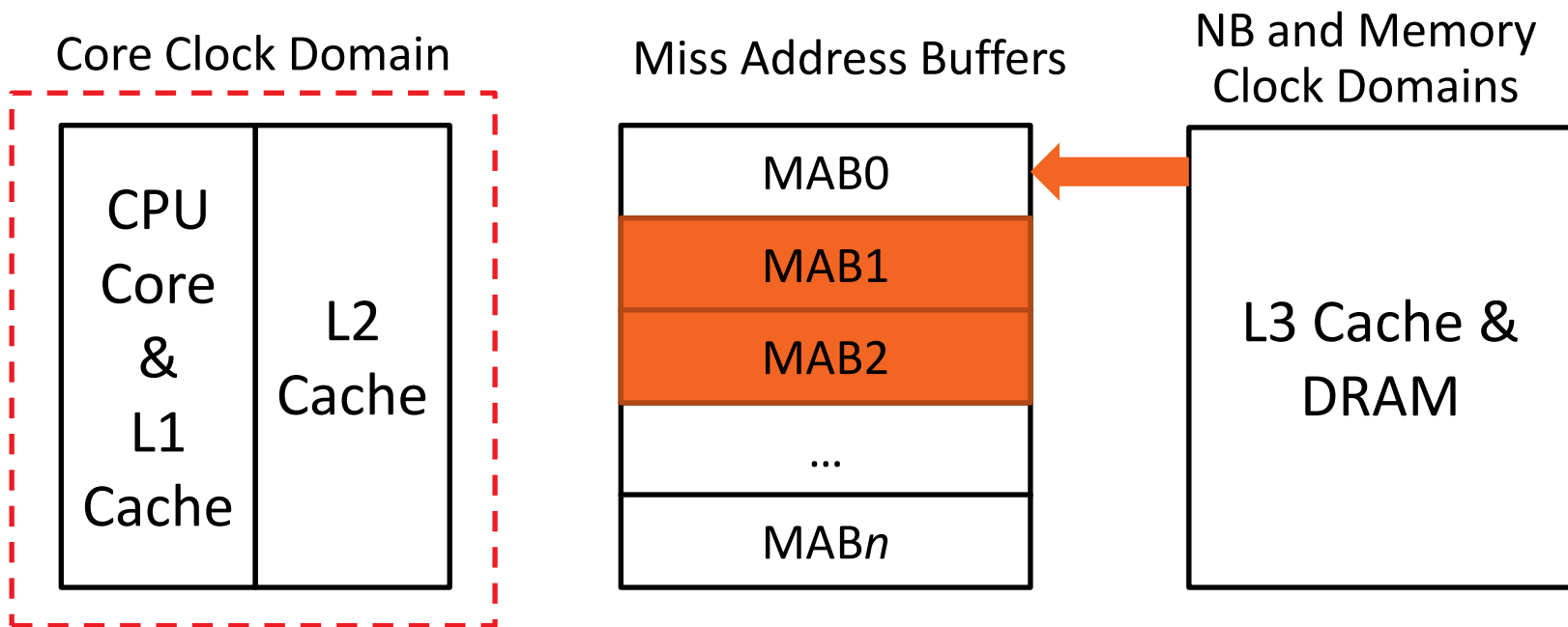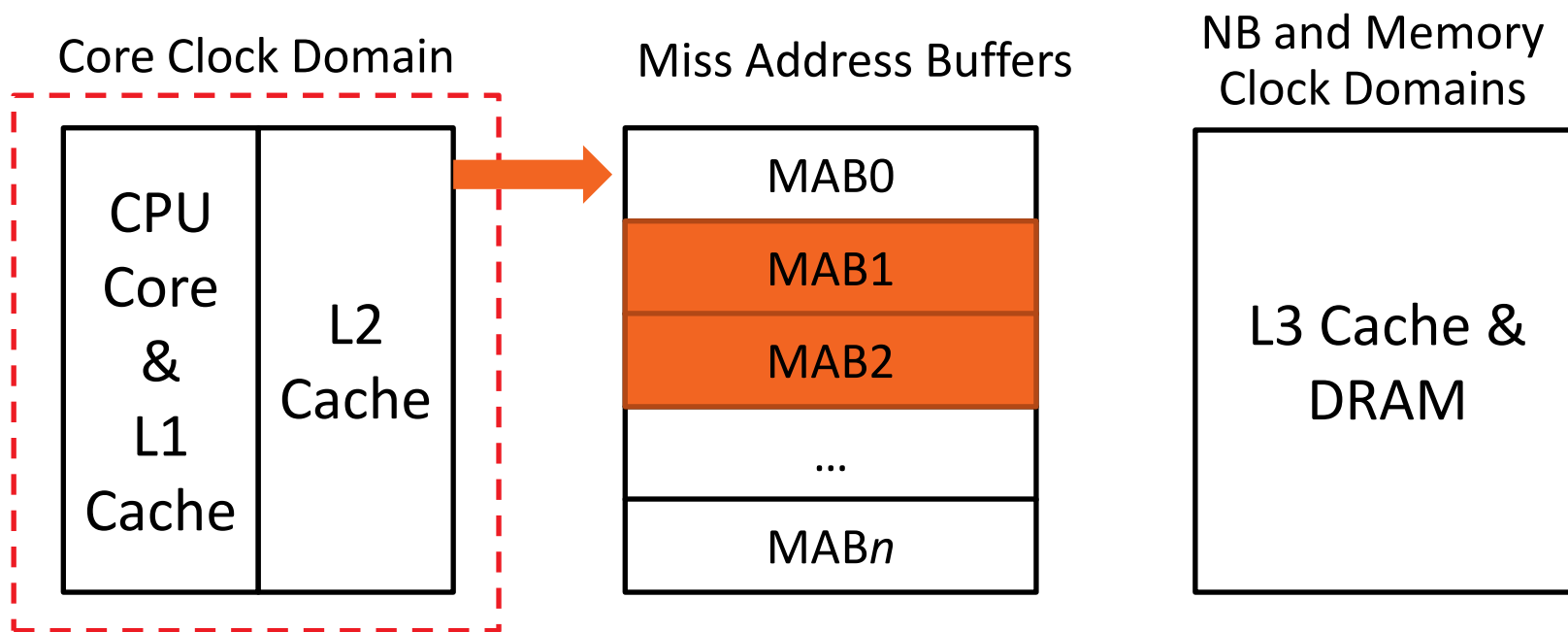**AMD**

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PERFORMANCE ESTIMATION MODEL: LL-MAB

Measure occupancy time of the highest-priority MAB
- HW event 1: CPU Clocks not Halted (for Execution Time)
  - Performance Event 0x76
- HW event 2: MAB Wait Cycles (for Memory Time)
  - Performance Event 0x69
  - Family 15h Processors: Unit Mask 0

$$Memory\ Time(f1) = MAB\ Wait\ Cycles(f1)/(f1)$$

$$Core\ Time(f1) = Execution\ Time(f1) - Memory\ Time(f1)$$

$$Execution\ Time(f2) = Core\ Time(f1) * f1/f2 + Memory\ Time(f1)$$

EVALUATING PERFORMANCE PREDICTORS

▲ Run benchmarks at frequency 1, estimate runtime at frequency 2

▲ Run benchmark at frequency 2.
 – Difference between observed and estimated is **estimation error.**

▲ Estimation mechanisms:
 – Linear: Performance scales exactly with frequency (like bzip2)
 – Green Governor:
   – Count L3 cache misses
   – Assign delay to each cache miss
   – # Cache Misses * delay = "memory time"
 – LL-MAB: Count MAB0 cycles at "memory time"

EXPERIMENTAL SETUP
OTHER PROCESSORS TESTED IN THE PAPER

AMD Opteron™ 4386 Processor
- 2nd Generation Family 15h "Piledriver" CPU
- Minimum Frequency: 1.4 GHz, Maximum non-boost frequency: 3.1 GHz

Fedora® 19 Desktop (kernel version 3.10.6-200)
- Locked benchmarks to single core with *numactl*
- Used *msr-tools* to read performance counters around benchmark runs.
- *CPUFreq* userspace governor to manually control DVFS state. Boosting disabled.
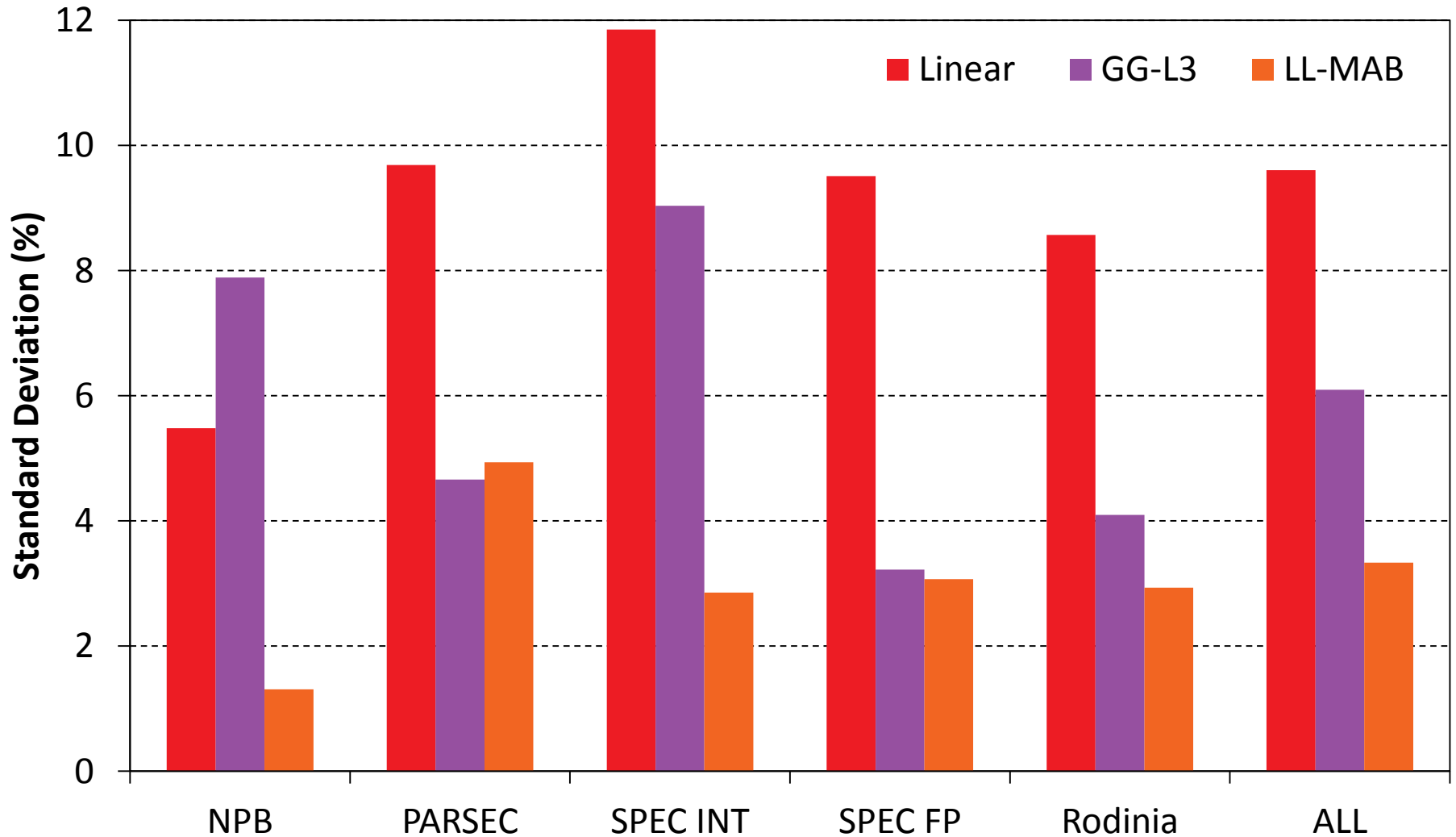
66 Single-threaded benchmarks from:
- SPEC® CPU 2006
- NAS Parallel Benchmarks
- PARSEC
- Rodinia

MEASURE AT 3.1 GHZ, ESTIMATE 1.4 GHZ RUNTIME
(LOWER IS BETTER)

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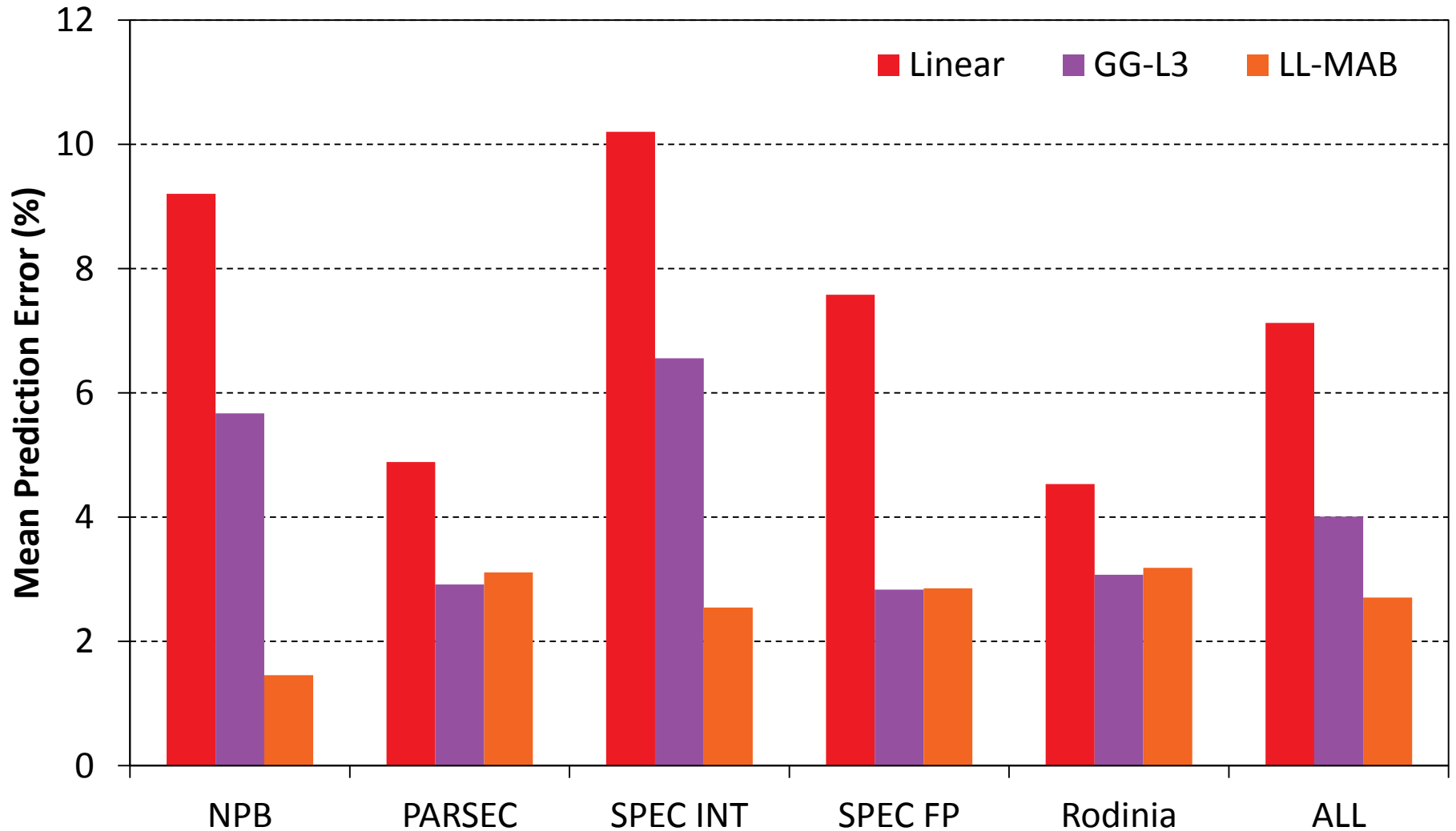
STANDARD DEVIATION IS IMPORTANT FOR PREDICTIONS AMD◢
(LOWER IS STILL BETTER)

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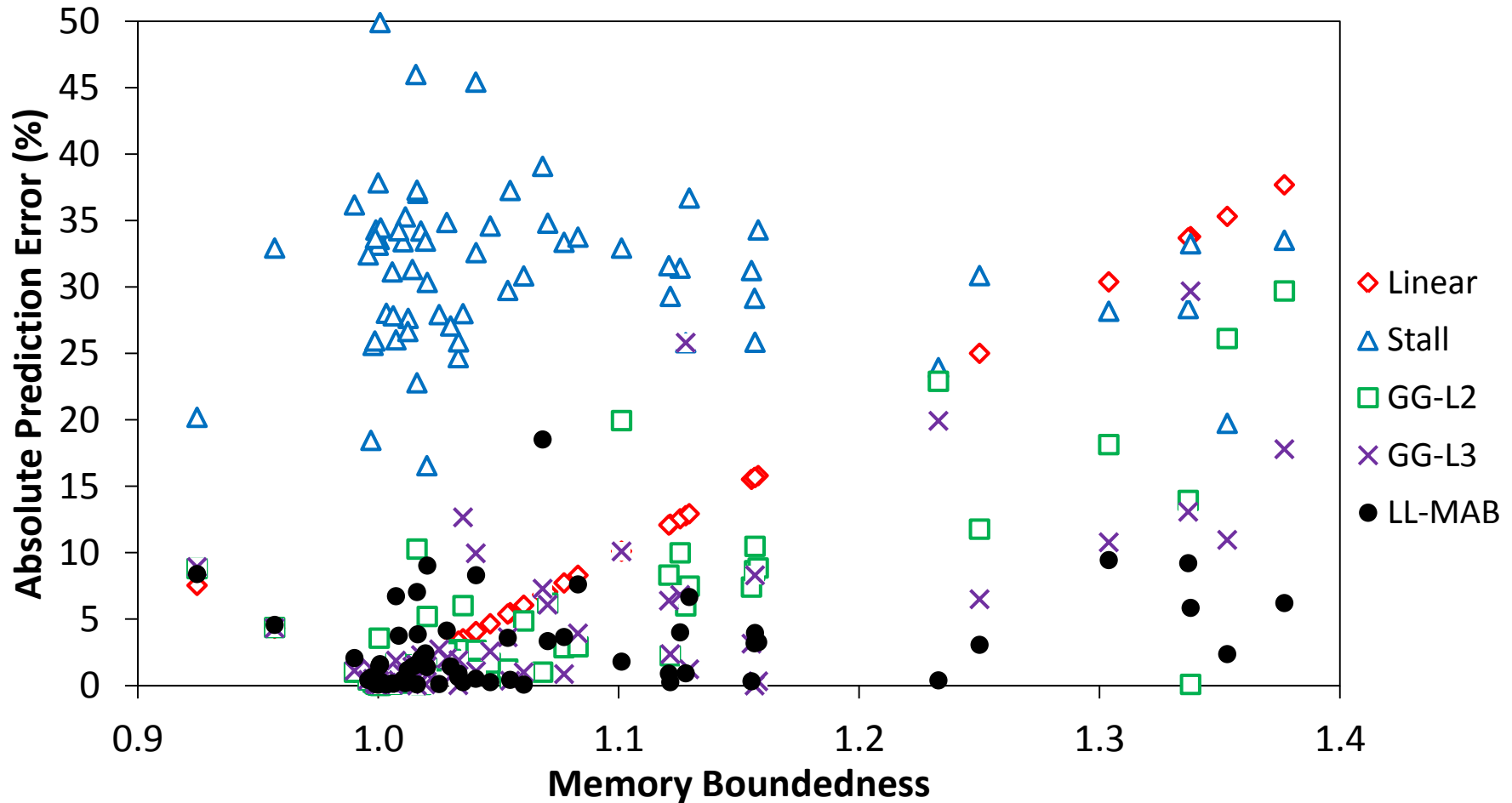
Backup Slides

PREDICTION ACCURACY PER BENCHMARK

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Memory Boundedness = Ratio of execution cycles at two frequencies

– 1.0 = no change in cycles (completely compute bound, e.g. bzip2)

CONCLUSION

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◢ First leading loads implementation on real processors

◢ Higher accuracy than existing predictors

◢ Lower accuracy than simulation due to HW complexity

◢ Lightweight estimation mechanism (only requires 2 counters)
   – Path to better performance and power prediction